(19) Japan Patent Office (JP)

(12) Publication of Laid-Open Patent Application (A)

(11) Publication No. 7-175038

(43) Publication Date: July 14, 1995

(51) Int. Cl.[6] Discrimination Mark:

G02F	1/133	550	
	1/136	500	
G09G	3/36		
H04N	5/66	102	B

FI

Request of Examination: Not filed

The Number of Claims: 4 (6 pages in total)

(21) Application No. 5-317221

(22) Filing Date: December 17, 1993

(71) Applicant: 000005049
Sharp Corporation
22-22 Nagaike-cho, Abeno-ku, Osaka, Japan

(72) Inventor : Naoyuki SHIMADA
c/o Sharp Corporation
22-22 Nagaike-cho, Abeno-ku, Osaka, Japan

(72) Inventor : Toshihiro YAMASHITA
c/o Sharp Corporation
22-22 Nagaike-cho, Abeno-ku, Osaka, Japan

(72) Inventor : Kimihide WATAYA
c/o Sharp Corporation
22-22 Nagaike-cho, Abeno-ku, Osaka, Japan

(74) Agent:

Patent Attorney: Masaru UMEDA

(54) [Title of the Invention] Driver circuit of display device

(57) [Abstract]

[Object] To provide a driver circuit of a display device in which wiring resistance is equalized with a simple constitution and without affecting various characteristics.

[Constitution] In a circuit constitution, a sampling gate 108 is connected between a video signal line 120 and a gate bus line 112, and the on/off control is carried out in accordance with a signal from a shift register. In connecting to the video signal line 120 through a connection electrode 4 and a connection wiring 1 on the side of a source electrode of the sampling gate 108, the connection is carried out with a connection point of a contact hole 5 at the connection electrode 4 shifted by a distance of a wiring pattern of a video signal line in order to equalize a relative distance L between connection points, that is between contact holes 2 and 5 each of which is a connection point, so that wiring resistance of a connection wiring can be equalized.

[Scope of Claims]

[Claim 1] A driver circuit of a display device comprising a circuit constitution in which a plurality of first signal lines which are wired in parallel and a plurality of second signal lines which are wired in parallel are connected to each other through a control means, and the control means connects each other by carrying out the on/off control by a third signal line separately,

characterized in that the connection is carried out at which a relative distance between a connection point at the control means and a connection point at each of the signal lines is the same.

[Claim 2] The driver circuit of a display device according to claim 1 characterized in that in connecting the first or second signal line to an electrode of a plurality of sampling gates which are control means through a connection wiring, a position of a connection point at an electrode of the sampling gate is changed in accordance with a position of a connection

point at the signal line so as to be the same distance.

[Claim 3] The driver circuit of a display device according to claim 1 characterized in that in connecting the first or second signal line to an electrode of a plurality of sampling gates which are control means through a connection wiring, the connection wiring is arbitrarily lengthened along a signal line, and a position of a connection point at the signal line is changed such that a relative distance from a connection point at the electrode of the sampling gate is the same.

[Claim 4] The driver circuit of a display device according to claim 2 or 3 characterized in that sheet resistance of the connection wiring has a resistance value which is more than double relative to sheet resistance at an electrode portion of the sampling gate.

[Detailed Description of the Invention]

[0001]

[Industrial Applicable Field] The present invention relates mainly to the improvement of a driver circuit used in a display device such as a liquid crystal display element.

[0002]

[Prior Art] FIG. 4 shows a TFT active-matrix liquid crystal display device which has been conventionally used. In this liquid crystal display device, a liquid crystal panel and a driver circuit are formed over the same substrate so that further reduction in size and weight is achieved compared with the conventional one, and it can be provided as an integrated type component as a display unit. Such a technology has already been adopted to known constitutions widely, needless to disclose in Japanese Patent Application Laid-Open No. 62-148928.

[0003] In the drawing, a liquid crystal panel 110, and a gate driver circuit 105 and a data driver circuit 106 which are provided at the length and breadth of the liquid crystal panel 110 respectively are formed over a substrate 100. The gate driver circuit 105 outputs a signal for controlling a TFT 114 to a gate bus line 111. When the TFT 114 is turned ON by this signal, a data signal supplied from the data driver circuit 106 to a data bus line 112 is written to a capacitor of a liquid-crystal pixel element and an additional capacitor of each pixel element (collectively denoted by a capacitor 113) to operate and control the liquid

crystal.

[0004] In the data driver circuit 106, the sampling gate 108 is controlled by an output of a shift register 107, and a video signal of RGB is supplied from outside through the video signal line 120 to flow into the data bus line 112 when the sampling gate 108 is ON, thereby the above-mentioned data signal is supplied.

[0005] FIG. 5 and FIG. 6 illustrate a cross-sectional diagram and a wiring pattern over the substrate of the periphery of the sampling gate 108 respectively.

[0006] In FIG. 5, a polycrystalline silicon layer 122 is formed over the substrate 100, which is a lower electrode of a semiconductor layer of a TFT constituting the sampling gate 108, and then patterned. Subsequently, a gate insulating film 123 is formed. A polycrystalline silicon layer 124 is formed and patterned, which is an upper electrode of a gate electrode of the TFT. After a doping step is performed by ion implantation into a predetermined portion, an interlayer insulating film 125 is formed over the entire surface to open a contact hole at the predetermined portion. A metal wiring 126 is formed and patterned. In addition, a second interlayer insulating film 127 is formed. Accordingly, a wiring pattern of the sampling gate 108 and the periphery thereof is formed over a glass substrate. Each of source electrodes of a plurality of the sampling gates 108 according to the above-described structure is connected to the video signal line 120 through a connection electrode 200 which is a metal wiring layer 126 (b) and a connection wiring 210 which is a polycrystalline silicon layer 124 (b).

[0007] FIG. 6 shows a wiring pattern to the video signal line 120 in each of the sampling gates 108. In the drawing, the video signal line 120 is formed by a metal wiring layer to connect to the connection wiring 210 through a contact hole 300. Furthermore, the connection wiring 210 is connected to the connection electrode 200 through a plurality of contact holes 301 and connected to a source electrode of the TFT constituting the sampling gate 108 through a plurality of contact holes 302. In the sampling gate 108, a signal line X1 to Xn on the side of a shift register which is a polycrystalline silicon layer 124 (a) is lead and the on/off control is carried out to connect to the data bus line 112 through a plurality of contact holes 303.

[0008] It is seen here that respective distances LL1 to LL3 of the connection wiring 210 between a connection point at each of the video signal lines 120 of RGB by the contact hole 300 and a connection point at the connection electrode 200 by the contact hole 301 differ depending on the sampling gate. In the case where the connection wiring 210 is formed of a polycrystalline silicon layer, sheet resistance thereof becomes large, and therefore respective wiring resistance differ largely with one another. Thus, when each of the sampling gates 108 is turned ON and the same video signal is supplied from the video signal lines 120, respective levels of video signals supplied to the data bus lines 112 differ, so that shading is generated. This phenomenon is recognized as vertical stripes in the case of a monochrome display in particular, and therefore, the image quality extremely deteriorates.

[0009] In addition, such a disadvantage appears as the phenomenon that in the case of adopting, in particular, a dot-sequential drive of storing signals in the capacitor of the source bus line 112 in which a signal is written to the source bus line which has relatively large capacitance, when the above-mentioned wiring resistance values differ, variation of a time constant due to them is generated to deform a waveform or stagger timing of a signal.

[0010]

[Problems to be Solved by the Invention] In order to prevent various phenomena which appear due to variations in wiring resistance as described above, a technology for equalizing wiring resistance can prevent of cause. For example, a technology for equalizing a resistance value by changing arbitrarily the width and the length of a wiring pattern to be connected is disclosed in Japanese Patent Application Laid-Open No. 5-72563.

[0011] In the drawing of FIG. 6 which is posed as a conventional example of the present invention as described above, wiring resistance is equalized and handled by narrowing the width of a wiring as for a short wiring to improve the sheet resistance value.

[0012] However, the above-mentioned method for changing a resistance value by the width of a wiring requires an ultrafine wiring in accordance with the advancement of a larger display screen and high definition nowadays, and it tends to be difficult to make difference of a resistance value as is conventionally done even from the viewpoint of pattern precision.

In addition, this has a problem of a mesh size of a design mask to generate a physical obstacle.

[0013] Furthermore, even when the above-described problems are cleared, equalization of wiring resistance is not necessarily easy because a slight deviation in the width of a wiring directly leads to a variation of a resistance value. Instead, in the case where the length of a wiring is lengthened as another method, there is such a disadvantage that space over a substrate is occupied due to corresponding distance and area required, and particularly in the case where the length of the wiring is lengthened by folding a pattern, line capacitance is generated due to a new pattern, thereby a characteristic is changed to generate a new variation.

[0014] The present invention is to provide a driver circuit in which these disadvantages are resolved and wiring resistance is equalized with a simple constitution and without affecting various characteristics.

[0015]

[Means To Solve the Problems] In order to achieve the above-described objectives, a driver circuit of a display device of the present invention comprising a circuit constitution in which a plurality of first signal lines which are wired in parallel and a plurality of second signal lines which are wired in parallel are connected to each other through a control means, and the control means connects each other by carrying out the on/off control by a third signal line separately, is characterized in that the connection is constituted at which a relative distance between a connection point at the control means and a connection point at each of the signal lines is the same.

[0016] In addition, it is characterized in that in connecting the first or second signal line to an electrode of a plurality of sampling gates which are control medium through a connection wiring, a position of a connection point at the electrode of the sampling gate is changed in accordance with a position of a connection point at the signal line so as to be the same distance.

[0017] In addition, it is characterized in that in connecting the first or second signal line to an electrode of a plurality of sampling gates which are constituted by a transistor and the

like and which are control medium through a connection wiring, the connection wiring is arbitrarily lengthened along a signal line, and a position of a connection point at the signal line is changed such that a relative distance from a connection point at the electrode of the sampling gate is the same.

[0018] It is also characterized in that an adverse effect due to the position change of a connection point is disregarded because sheet resistance of such a connection wiring has a resistance value which is more than double relative to sheet resistance at an electrode portion of a sampling gate.

[0019]

[Influence] According to the present invention, a connection distance from the viewpoint of an interval of connection points is the same, and therefore, change of the pattern width or the like in order to equalize wiring resistance as is conventional is not required at all. A technology for handling only by changing a connection position can be controlled with relatively high precision even at the present level of technology, so that a variation in wiring resistance can be reduced to the almost trouble-free level. Such a change can be carried out at low cost and with ease, which is out of sight in the conventional technology as well.

[0020]

[Example] One example of the present invention is explained below in accordance with FIG. 1. The drawing shows a magnified diagram of a wiring pattern of a sampling gate and the periphery of a video signal line. A manufacturing procedure and a constitution of a display device of the portion not described in this example are similar to the conventional example. In addition, the portion having the identical constitution is denoted by the same reference numerals as the conventional example.

[0021] In the present example, the connection electrode 4 of the source electrode of the sampling gate 108 which is configured by a TFT and the video signal line 120 are connected to each other by the connection wiring 1. The connection wiring 1 is formed by the polycrystalline silicon layer (124) formed at a thickness of 450 nm doped to be N-type, and the sheet resistance value thereof in this case is 30 Ω. A metal wiring layer of Al formed at a thickness of 400 nm is employed as the video signal line 120 for supplying

video signals, and the sheet resistance value thereof in this case is 0.1 Ω.

[0022] Respective connection wirings 1 which connect the sampling gates 108 and the video signal lines 120 to each other are formed by the above-mentioned polycrystalline silicon layer. This connection wiring 1 is connected to the video signal line 120 through a contact hole 2. The source electrode of the sampling gate 108 is connected to the connection electrode 4 formed by a metal wiring layer through a contact hole 3 and connected to the connection wiring 1 through a contact hole 5.

[0023] There are six connection points by this contact hole 5, for example, and on a sampling gate side at the left end, when connecting to the lowest line 120R of the video signal line 120, the connection points by the contact hole 5 are placed at the lowest position so that a distance between connection points is L.

[0024] Similarly, on a sampling gate side at the middle, when connecting to the middle line 120G of the video signal line 120, which brings an upward shift by space of a wiring pattern of the video signal line 120, and thus the connection points by the contact hole 5 are shifted in the upward direction by the space of the wiring pattern so as to be equalized to the distance L between connection points at the above-mentioned left end.

[0025] Similarly, on a sampling gate side at the right end, when connecting to the uppest line 120B of the video signal line 120, which brings a further upward shift by space of a wiring pattern of the video signal line 120, and thus the connection points by the contact hole 5 are shifted in the upward direction by the space of the wiring pattern so as to be equalized to the distance L between connection points at the above-mentioned left end and middle. That is, this technology is to make a distance L constant by shifting connection points by the contact hole 5 on the sampling gate side by a distance between wirings of the video signal line, so that wiring resistance is the same.

[0026] According to the above-described constitution, because a positional relationship between connection points by the contact hole 5 and the connection electrode 4 differs with sampling gates, it seems that a new problem may arise. However, when the connection electrode 4 is formed by a metal wiring layer and the sheet resistance thereof is made to have a resistance ratio 1/300 of a gate layer constituting the connection wiring 1, it is

possible to suppress variations of a resistance value over the connection electrode 4 due to the change of the position of the contact hole 5 to the virtually negligible level.

[0027] Another example of the present invention is shown in FIG. 2. The drawing shows a magnified diagram of a wiring pattern of a sampling gate and the periphery of a video signal line as is in FIG. 1.

[0028] The present example is effective in the case where contact holes can not be shifted within the sampling gate described in the preceding example by a distance of a wiring of a video signal line. That is, the connection wiring 1 for connecting the sampling gate 108 and the video signal line 120 to each other is connected to the video signal line 120 through the contact hole 2 and connected to the connection electrode 4 through the contact hole 5. To equalize a distance between connection points by these contact holes 2 and 5, the connection wiring 1 is extended on the video signal line 120 and a position of the connection point by the contact hole 2 is changed to be at the connection wiring.

[0029] That is, without changing the contact holes 5 on the gate electrode 4 in the respective sampling gates, on a sampling gate side at the left end, in connecting to the lowest line 120R of the video signal line 120, the connection wiring 1 is arranged vertically as it is because its position is located in the farthest position and connected as it is at the position crossing the video signal line 120R (a position at which a relative distance from the contact hole 5 is L) by the contact hole 2.

[0030] Next, on a middle sampling gate, in connecting to the middle line 120G of the video signal line 120, the connection wiring 1 is folded along the video signal line 120 and connected to the video signal line 120G by the contact hole 2 whose position is a top end of the folded portion and a position at which a relative distance from the contact hole 5 is L.

[0031] Furthermore, on a sampling gate at the right side, in connecting to the uppest line 120B of the video signal line 120, the connection wiring 1 is folded farther along the video signal line 120 and connected to the video signal line 120B by the contact hole 2 whose position is a top end of the folded portion and a position at which a relative distance from the contact hole 5 is L.

[0032] Therefore, according to each of the examples, a distance of a connection wiring

between connection points is completely the same, which can completely solve the problems due to difference in wiring resistance.

[0033] The above-described examples each discloses a constitution for a connection to a video signal line in a sampling gate in order to equalize wiring resistance. However, this invention is not limited thereto and is applicable to another circuit portion having a common problem. FIG. 3 illustrates a wiring pattern on a clock input side of the shift register 107 in the circuit constitution diagram shown in FIG. 4. Two blocks of a shift register are operated by four phases of a clock signal here. The drawing shows a layout of the periphery of a clocked inverter to which the clock signal is input.

[0034] As shown in the drawing, a distance to a TFT 510 differs with variety of a clock wiring 500, and therefore difference in wiring resistance is generated in the case of a conventional wiring, which staggers timing of sampling in the two blocks of the shift register and becomes a cause of a display variation. However, the wiring is folded along a clock signal line so that the distance to a connection point at each of the TFT 510 is relatively the same, and a connection point is arranged at the top end thereof. According to such a constitution, a sampling stagger in each of stages of the shift register can be prevented and display quality can be improved.

[0035]

[Effect of the Invention] As hereinabove, according to the present invention, connection distances from the viewpoint of between connection points are equalized by changing only a position of a connection point, and therefore, change of the pattern width or the like in order to equalize wiring resistance as is conventional is not required at all and no space for a farther wiring distance is required. Therefore, deterioration of display quality due to a variation of a pattern or generation of floating capacitance does not appear, and a quite effective driver circuit of a display device can be realized with a simple constitution.

[Brief Description of the Drawings]

[FIG 1] a plan diagram showing one example of a wiring pattern of a driver circuit of a display device of the present invention.

[FIG 2] a plan diagram showing another example of a wiring pattern of a driver circuit of a

display device of the present invention.

[FIG 3] a plan diagram showing another usage example of a driver circuit of a display device of the present invention.

[FIG 4] a constitutional diagram of a main circuit of a TFT active-matrix liquid crystal display device.

[FIG 5] a cross-sectional diagram of a circuit board in the periphery of a sampling gate.

[FIG 6] a plan diagram illustrating a wiring pattern of a driver circuit of a conventional display device.

[Explanation of the reference numerals]

1: connection wiring

2: contact hole

3: contact hole

4: connection electrode

5: contact hole

108: sampling gate

112: data bus line

120: video signal line

L: distance of wiring between connection points